Remarks

Acceptance of this response and favorable action therefor of the above-identified application is respectfully requested.

With the above made amendments, claims 1, 9, 11, 22 and 23-26 remain pending of which claims 1 and 9 are currently amended and claims 23-26 are newly presented. The changes implemented in independent claims 1 and 9 are strictly of a grammatical nature. Newly presented independent claims 23 and 25 are based on the subject matter covered by pending claims 1 and 9, respectively, but without the additional featured aspect directed to the thickness of the set forth "first insulating layer" of claim 1 or that of the set forth "insulating layer" according to claim 9. Newly presented claims 24 and 26 which are combined with claims 23 and 25, respectively, are based on claims 22 and 11, respectively.

As will be shown by the rebuttal arguments in conjunction with the accompanying Declaration under 37 CFR §1.132, by the inventor, a thin-film transistor according to claims 1+ and 9+ and, further, according to newly added claims 23-26 could not have been anticipated by Abe et al nor by Yamazaki et al. Though the previously standing rejection in view of Yamazaki et al was withdrawn by the Examiner, the inventor, nonetheless, has established (as a result of experimentation) that Abe et al's thin-film transistor and Yamazaki et al's thin-film transistor are structured differently from that of the present invention for at least the reasons that their TFTs require a differently structured glass substrate than that called for by the present invention. Accordingly, the outstanding rejection under 35 USC §102(b) in view of Abe et al (JP 8-195494) (and also in view of Yamazaki et al, insofar as applicable to the presently pending claims) is traversed, and reconsideration and withdrawal of the same is respectfully requested.

The invention according to claims 1+, and 23+ is directed to a thin-film transistor which includes a particularly structured glass substrate and formed at an upper part thereof are a channel region, a source region, a drain region, a first insulating layer and a second insulating layer, in which the first insulating layer covers the channel region and the second insulating layer, in turn, is formed on a surface of the first insulating layer. With regard to claims 9+ and 25+, rather than setting forth first and second insulating layers, the invention therein sets forth an insulating layer. An example illustration covered by the present invention can be seen with regard to the Fig. 1 embodiment, although not limited thereto. In the example Fig. 1 embodiment, a polycrystalline silicon layer (film) is used to form the source region 8, the drain region 9 and the channel region 12 and the insulating layers 6a and 6b are example illustrations of the first and second insulating layers of the TFT according to the invention.

According to a featured aspect of the invention in each of independent claims 1 and 23 as well as in independent claims 9 and 25, the set forth "glass substrate" has a structure whose characteristic physical properties are clearly different from that of a glass substrate required by Abe et al. This is similarly the case with regard to Yamazaki et al. Specifically, each of the independent claims 1, 9, 23 and 25 sets forth a **glass substrate** which is "*defined as having a physical property such that the compaction is 30 ppm or higher, when said glass substrate is heated at 600 ° C for 1 hour and thereafter cooled at a rate of 1° C/minute.*" This expression, it is submitted, pertains to the physical properties of the glass substrate itself and therefor is defining of the glass substrate structure. (The presently set forth expression in each of the independent claims, regarding the structural aspects of the glass substrate, is in keeping with the earlier understanding reached with the Examiner during the personal interview held with him on July 21, 2003 (see the

Examiner's comments in the continuation sheet of the Interview Summary record (form PTO-413) and the follow-up discussion in the Remarks of the Supplementing Amendment filed on July 28, 2003.) That is, the set forth expression, it is submitted, is a structurally defining aspect pertaining to the "glass substrate" called for according to the present invention. The glass substrate structure such as set forth in each of independent claims 1, 9, 23 and 25 defines an unannealed glass substrate (see page 5, lines 8-14, of the Specification).

Applicants have achieved a scheme by which a thin-film transistor (TFT) with an active region formed of polycrystalline silicon material to achieve greater electron mobility in the transistor (over that employing an amorphous silicon layer) can be manufactured under low-temperature processing conditions using an inexpensively made glass material as a substrate, in which, also, the threshold voltage remains stable. A glass substrate used in a TFT according to the present invention is a grown glass substrate that was not subjected to a pre-heating process prior to its use in the manufacture of a TFT.

In the example first embodiment of a TFT of the present specification, which uses a glass substrate according to that of independent claims 1, 9, 23 and 25, since the temperature processes involved in the manufacture thereof only reach about 450° C such as in connection with the formation of the insulating oxide film(s), the compaction (heat shrinkage rate) of the glass substrate is not adversely affected. *Generally, in the manufacturing process of a liquid crystal display panel using TFT technology, it is common knowledge that in the construction of a process design, deformation (e.g., heat shrinkage or compaction) of a glass substrate to be used should be restrained to 10-20 ppm, which is measured in terms of the alignment accuracy of the pattern mask.* This is explained in *A Handbook on Liquid Display Panel Manufacturing Technique*, page 193, 1992, published by Science

Forum, a copy of which is attached hereto [a copy of the same was also submitted earlier as an attachment to the Amendment of December 19, 2002]. Since the processes employed in the formation of the TFT according to the present invention involve temperature conditions considerably lower than the strain point of a glass substrate whose structure is that as presently defined in claims 1, 9, 23 and 25, which is characteristically an unannealed glass substrate, the compaction rate associated therewith is maintained at a very acceptable range.

It is submitted, due to its lower strain point, that is a temperature at which the compaction rate begins to increase considerably (causing deformation), a glass substrate with a structure as that defined in the claims cannot be used to achieve a TFT construction such as that taught by Abe et al or, for that matter, Yamazaki et al, both of which employed process temperatures in the formation of the TFT considerably higher than that employed by the present inventors. It is submitted, also, both Abe et al and Yamazaki et al used glass substrates that have undergone a heating process after they were grown at the manufacturer to raise the strain points so that significant or accelerated compaction rates begin at much higher temperatures. For example, the glass substrate employed in Abe et al must be able to withstand processing temperatures of up to 600 ° C without significant heat shrinkage (low compaction rate). This is similarly the case with Yamazaki et al. In accordance with the present invention, a processing temperature of 600 ° C with regard to the manufacture of the TFT would lead to a compaction (e.g., heat shrinkage rate) that is "30 ppm or higher," which is unacceptable and would lead to a defective product. In other words, the glass substrate according to the present invention, it is submitted, is different in structure from the glass substrate of the manufactured TFT according to Abe et al or, for that matter, according to Yamazaki et al.

In order to prove that the "glass substrate" according to claims 1+, 9+, 23+ and 25+ is a different structure than that required by Abe et al as well as Yamazaki et al to construct a TFT and, therefore, also show that a TFT realized according to the present claimed subject matter is structurally different from that disclosed or even suggested by Abe et al or, for that matter, by Yamazaki et al, the present inventor (in keeping with the earlier understanding reached with the Examiner in the personal interview held with him) is submitting herewith a supportive Declaration directed thereto based on the experimental results achieved with regard to four (4) experiments performed. The experiments are described in part **I** of the Declaration, titled *Experiments* and the results of which are discussed in parts **II** and **III** thereof.

Experiment No. 1 is directed to the manufacture of a TFT based on the first example embodiment of the present application. Incidentally, in the first, second and third experiments described in part I of the Declaration, the grown glass substrate used towards the manufacture of the TFT was one under the trade name of Corning 7059 which was not subjected to any heating process prior to the manufacturing process of the TFT. In *Experiment No. 1*, the laser annealing portion of the process, which did not lead to high temperature at the substrate, crystallized the amorphous silicon layer to form a polycrystalline silicon layer; the polycrystalline silicon layer was then patterned in which case alignment marks were formed for aligning a mask and the distances between the alignment marks in both the x- and y- directions were measured and are referred to as distances X1, Y1; the method then called for oxidizing the surface of the polycrystalline silicon layer which led to the formation of an SiO_2 film (or "first insulating layer") having a thickness of 10 nm, employing process temperature of 450° C for 30 minutes (step d); then a second SiO_2 layer (or "second insulating layer") having a thickness of 90 nm was formed by a plasma-CVD method (step e); this was followed by steps (f), (g) and (h), in that

order. (Related discussion regarding, especially, steps (d) and (e), which involve heat processes (in the manufacture of a TFT) impacting the glass substrate, are discussed in the second paragraph of page 9 of the original Specification. Regarding the choice of the first insulating film thickness to be 10 nm, this is keeping with the findings shown in Fig. 3 of the drawings and discussed on page 10, second and third paragraphs, of the Specification, which shows that the film thickness of the first oxide layer 6a should be at least 4 nm (e.g., 4 nm-20 nm) in order to ensure a flat-band voltage, which leads to desirable transistor characteristics.)

In *Experiment No. 2*, Yamazaki et al's oxide film forming process was instead used in the formation of the gate insulating film in the TFT manufacturing scheme. Specifically, in place of steps (d) and (e) in *Experiment No. 1*, the oxide film forming process employed by Yamazaki et al was used. With regard to *Experiment No. 3*, Abe et al's oxide film forming process was used instead for steps (d) and (e) in *Experiment No. 1*. *Experiment Nos. 2 and 3* were implemented to confirm that a glass substrate whose structure is characterized by a physical property as that of the present invention cannot be used in the manufacture of a TFT where the gate insulating film processes involve temperatures considerably higher than that in *Experiment No. 1.* In that regard, process temperatures employed in the formation of the gate insulating oxide films in Yamazaki et al reached as high as 550 ° C and that in Abe et al reached temperatures as high as 600 ° C.

A further experiment was also performed by the present inventor, namely, *Experiment No. 4*, in which the process in *Experiment No. 1* was modified. Namely, in place of the glass substrate used in *Experiment No. 1*, which was not subjected to any prior heating process (i.e., an unannealed glass substrate), a commercially available Corning 7059 glass which was previously subjected to heat treatment by

the manufacturer was instead used. In other words, a commercially available annealed glass substrate was used. Also, in place of the process steps (d) and (e) in *Experiment No. 1*, Yamazaki's process for forming the oxide gate insulating film was employed. Said differently, *Experiment No. 4* is the same as that of *Experiment No. 2*, except for using an annealed glass substrate in place of an unannealed glass substrate. (Experiment Nos. 1, 2, 3 and 4 are fully described on pages 3- 5 of the accompanying Declaration.)

The results of the above four experiments are explained in part **II** of the accompanying Declaration in conjunction with the chart shown in **Appendix A** at the end of the Declaration. Specifically, both the flat band voltage (V_{FB}) as well as the glass compaction directed to each of the four experiments were measured since these characteristics directly affect reliability/effectiveness of the manufactured TFT. These measured characteristic values are explained on pages 6-7 of the Declaration. The distances between the alignment marks measured at the end of each of the above four experiments (i.e., after completion of step (h)) were set as distances X2, Y2. These distances X2, Y2, measured after each experiment, were compared with the corresponding measured distances X1, Y1, at step (c) of each experiment, to determine the glass compaction, which is defined as (X1-X2)/X1, (Y1-Y2)/Y1. The chart in Appendix A gives the measured values as it relates to each of the four experiments. The summary of the experimental results, which are shown in Appendix A, and conclusions reached therefor is given in part **III**.

As can be seen from the results in Appendix A, *Experiment No. 1*, directed to the present invention (in which the glass substrate used was not subjected to a heating process at the manufacturer [prior to its use in manufacturing the TFT], consistent with that called for in each of independent claims 1, 9, 23 and 25), achieved very favorable results in terms of its heat shrinkage (compaction rate) as

well as the measured V_{FB}. The favorable results regarding the compaction rate allows for the formation of additional layered patterns to be formed within design permissible values. That is, a TFT manufacturing process employing a heating history that is not raised, for example, beyond about 450 ° C or slightly higher, affords the use of a glass substrate whose structure is defined by a physical property as that mentioned above, consistent with that set forth in independent claims 1, 9, 23 and 25. As earlier mentioned, with regard to TFT technology such as used in manufacturing processes of LCD panels, deformation (e.g., heat shrinkage or compaction) of a glass substrate to be used therein should be restrained to 10-20 ppm, which is measured in terms of the alignment accuracy of the pattern mask.

Also from the results achieved, a glass substrate according to the present invention such as that used in *Experiment No. 1* would not achieve favorable results if it is employed under TFT heat processing conditions as that used by Yamazaki et al (*Experiment No. 2*) and Abe et al (*Experiment No. 3*). With regard to *Experiment No. 2*, which employed Yamazaki et al's silicon oxide film forming processes, which reached temperatures as high as 550° C, the results in **Appendix A** show that an excessively high heat compaction rate of 60 ppm developed in the glass substrate, which is way outside the permissible deformation amounts for glass substrates. In fact, the results achieved were even more unfavorable when it came to employing a glass substrate structure according to the present invention in the formation of TFT gate insulator films using Abe et al's silicon oxide film forming process, which required temperatures as high as 600 ° C. For example, the heat compaction rate of an unannealed glass substrate used in *Experiment No. 4* in the formation of a TFT, which employed the silicon oxide film forming process taught by Abe et al, reached to 90 ppm which relates to a deformation far greater than that of Yamazaki

et al's scheme. It is stated in the Declaration, in the paragraph bridging pages 8-9 thereof, that "*[t]hese values are way outside of the permissible deformation amounts for glass substrates. This is evidenced by the fact that it was impossible to achieve an accurate alignment of a pattern mask and, as a result, the TFT could not be reliably manufactured.*"

In *Experiment No. 4*, the same process as that according to *Experiment No. 2* was employed, except the inventor made a substitution in the type of glass substrate used. That is, with regard to experiment number 4, rather than employing a previously unheated grown glass substrate (i.e., an unannealed glass substrate), an annealed glass substrate was instead used (i.e., a glass substrate that was involved in a heating process after it was grown at the manufacturer but prior to its use in a TFT manufacturing scheme). From the results achieved, which are applicable to both the glass substrate employed in Yamazaki et al as well as in Abe et al, it is noted that the compaction rate of the annealed substrate, according to Experiment No. 4, "*was so restrained that it could very safely withstand a normal (i.e., conventional) TFT manufacturing process (e.g., a process involving temperatures of 600 °C or lower" without any problem),*" the inventor submits (see page 9, lines 11-14, of the Declaration).

Other than the type of glass substrate employed, the inventor noted (in the Declaration), there were no further differences between the process involved in *Experiment No. 2* and that in *Experiment No. 4*. However, unlike the results of *Experiment No. 2*, "*the process of manufacturing a TFT according to Experiment No. 4 obtained very favorable results in terms of the glass compaction and the flat band voltage*," the inventor observed (see Appendix A and the last paragraph on page 9 of the Declaration). Moreover, even though the high process temperatures of 550 ° C and 660 ° C of *Experiment Nos. 2* and *3* led to an excessive deformation

amount when the glass substrate employed had a structure consistent with that defined in claims 1, 9, 23 and 25, such excessive deformation did not occur when the glass substrate used was instead of an annealed type (see the results of *Experiment No. 4*). The results achieved with regard to *Experiment No. 4* included "a very acceptable [compaction] rate of 6 ppm and ...a flat band voltage of about 0V, which is considered excellent," the inventor observed (see Appendix A and page 10, paragraph 1 of the Declaration).

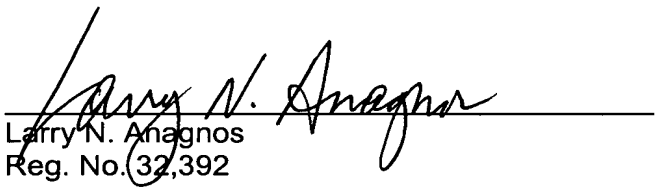
From the experimental findings, which are summarized in Appendix A, the inventor concludes, employing a glass substrate of the type having physical properties consistent with that of the present invention does achieve satisfactory results when used in a manufacturing scheme under heat processing conditions of *Experiment No. 1*, which is based on the method to achieve the TFT of the present invention. However, with regard to manufacturing schemes such as that employed by Abe et al or Yamazaki et al, which formed the oxide insulating layers under much higher temperature processing conditions (see *Experiment Nos. 2* and *3*), a glass substrate that has not undergone an annealing process beforehand could not have led to the successful manufacture of TFTs. The inventor submits, consistent with his findings, which are summarized in Appendix A, "a glass substrate whose structure is defined by a physical property as that according to the present invention ..., cannot be employed in the TFT process according to Yamazaki et al and Abe et al," (see page 11, first paragraph, the last sentence thereof). On the other hand, favorable results were achieved under such high temperature processing conditions when the glass substrate used was an annealed substrate. That is, the inventor confirmed that under temperature processing conditions as high as 600 ° C, in the formation of TFT SiO_2 insulating films, the glass substrate must have a physical property in which the compact rate is substantially lower than 30 ppm to avoid

pending claims, i.e., claims 1, 9, 11 and 23-26, and an early formal notification of allowability of the above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by a personal interview, the Examiner is invited to contact the undersigned representative at the number indicated below.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (566.40894X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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Enclosures:
Declaration Under 37 CFR §1.132 (incl. Appendix A)